

The resultant degradation in ST_B/N_0 due to subcarrier phase noise is shown in Fig. 24 as a function of ST_B/N_0 for data rates of $8\frac{1}{3}$, $33\frac{1}{3}$, $66\frac{2}{3}$, and 270 bits/s.

B. Communications System Research

1. Mariner Venus 67 Ranging System Digital Processing

Design, W. A. Lushbaugh and L. D. Rice

a. Introduction. This article describes the design of the digital processing portion of the *Mariner Venus 67* ranging system. For a discussion of the entire ranging system, see SPS 37-42, Vol. III, pp. 52-56. A general functional description of the system is given in the following Paragraph b.

The use of a digital computer for correlation and decision functions greatly enhances the flexibility of the ranging system. However, it also introduces a number of problems due principally to the discrete nature of the information involved in the range measurement, and to the different time scales upon which the computer and the various subsystems operate. This article discusses several specific problems, and their various solutions, encountered in the design of the digital hardware/computer software interface. For a detailed description of the digital and software portions of the system, see the following two articles, subsections B-2 and B-3, respectively.

b. Ranging system functional description. Figure 25 shows that the system consists of a number of RF, digital, and computer software subsystems that interact to perform the functions of range and range-rate calculations. Received signal, reference tones, and an RF doppler signal pass from the DSIF receiver to the analog portion of the system where the product of the received signal with the ranging system receiver coders is generated and filtered. The signals then pass through the digital interface equipment to the SDS 920 computer, which computes the correlation and acts to systematically align each of the six code components with the code contained in the received signal. While the correlations are being performed, the RF doppler signal is counted and used to correct the receiver coders for rate variation in the incoming signal. Once the receiver coders are aligned with the code in the received signal, the rate variations in the incoming signal are tracked by means of the code correlation itself. The range and range-rate are thenceforth available for output.

c. Programming problem areas. The ranging system, as seen by the computer program, is essentially a number of

distinct but related tasks that must be managed simultaneously. Because the digital computer is a sequential machine, the main problem is the establishment of correct timing relationships between system component operation and computer program execution.

The most critical problem, with respect to timing considerations, is that of maintaining phase-locked synchronization of the doppler-aided tracking loop with the clock doppler frequency, which is centered around 100 ± 70 Hz. Thus, the loop must be phase-locked over this frequency range. This is accomplished by checking the phase relationship once each cycle and updating the cycle time of the number-controlled oscillator (NCO) to maintain the correct phase. The two routines that check the phase relationship (PHDINT) and control the NCO (NCOINT) are described in the article by D. L. Rice appearing in this volume. Controlling the timing of the NCOINT routine is accomplished by an interrupt signal generated each time the NCO counts down one cycle. The phase-detector counter is also started at this time. The counter is stopped on the next cycle of the clock doppler frequency, which also generates an interrupt to execute the PHDINT routine. The phase-detector counter is then read and reset by PHDINT.

A difficulty arises from the possibility that if the loop frequency and the clock doppler frequency are not identical, two successive cycles of one frequency can occur before the next cycle of the other frequency. In one case, the counter will be read before it has been started by the NCO, and in the other case, the counter will be restarted before it has been read and reset. Either case results in an erroneous count.

This problem is solved by disarming the PHDINT phase-detector routine inside itself so that once it has been executed, the interrupt will not respond until it has been rearmed. This rearming is done in the NCO routine so that the PHDINT routine will be active only once after each execution of NCOINT. Making the NCOINT a higher priority than the PHDINT assures that any phase shift input to the NCO will be entered into the loop only once.

Another timing problem is related to the use of the typewriter under interrupt control so that main program operation is delayed for the shortest possible time. A queue is established by setting a flag corresponding to each output message desired. These flags are checked once each second to determine whether any messages are waiting to be typed. An alternate method is to construct a list of waiting messages and type from this list if it is

non-empty. This system requires either a much more elaborate memory allocation scheme than is used, or an absolute limit to the number of messages waiting for type-out. In the latter case, if the list is full, a message may be ignored entirely. In the system as used, a message request may be ignored if the corresponding flag is already set, but each message requested will eventually be typed at least once. When a message is set up for typing, its flag is reset and it may then be requested again.

d. Hardware synchronizing problem. The SDS 920 is a synchronous machine with a basic timing cycle of $8 \mu\text{s}$. The special-purpose digital equipment added to it for the *Mariner Venus 67* ranging experiment was tied to a 1-MHz standard clock or the 500-kHz plus clock doppler frequency. The synchronizing problem was two-fold since both the computer and digital rack command each other at various times in the ranging operation. A special synchronizing circuit was developed for each of these timing problems (refer to the article by W. A. Lushbaugh appearing in this volume).

e. Hardware/software optimization. In a few instances, the close cooperation of the logic designer and programmer led to a system simplification. For example, each of the various binary counters in the digital rack had to be frozen at the 1-s time tick and read into the computer. It was thought originally that two counters would be needed in each case with each used on alternate seconds. By proper arrangement of interrupt priorities, however, it was arranged to have only a small auxiliary counter to count events while the computer was reading the main counters (see the article by W. A. Lushbaugh appearing in this volume).

Another interesting hardware/software trade-off was made in the design of the NCO. During the design of this oscillator, it became obvious that a saving of hardware would result if an extra clock period was used to develop the transfer of the desired number from its hold register to the binary counter. Doing this and re-interpreting the definition of binary *one* in the hold register meant that the programmer could use *two's* complement for the desired period. Since programming the desired period in *two's* complement form was easily introduced, this format was adopted.

2. Mariner Venus 67 Ranging System Digital Rack,

W. A. Lushbaugh

a. Introduction. The *Mariner Venus 67* ranging system (see Ref. 1 and SPS 37-42, Vol. IV, pp. 198-200) uses a

rack of special-purpose digital equipment to relieve the computer of some necessary bookkeeping functions. This equipment is in addition to an SDS 920 computer, an RF rack, and digital-to-analog and analog-to-digital converters (see SPS 37-48, Vol. II, pp. 63-67). The digital rack was constructed with standard modules and comprises approximately eight rows of 25 modules each. The digital rack is actually a set of subsystems that fit into various parts of the tracking loop.

The main blocks are as follows:

- (1) Computer output interface
- (2) Transmitter and receiver code generators
- (3) Receiver coder output control
- (4) One-second interrupt time routine
- (5) Clock doppler counter
- (6) Fractional cycle counter
- (7) Number-controlled oscillator (NCO)
- (8) Digital phase detector
- (9) Ultra-high frequency (UHF) doppler counter

This article discusses each of these digital blocks.

b. Computer output interface. Since the basic purpose of the digital rack is to extend the capabilities of the SDS 920 computer, there is a great deal of communication between the two devices. Communication between the two systems is via the standard parallel input (PIN) connector, the parallel output (POT) connector, as well as various interrupts, and the \bar{S}_{sc} line (SKS instruction test line). The computer commands the digital rack by going through an EOM instruction followed by either a PIN or POT instruction while the digital rack commands the computer via the interrupt lines.

A block diagram of the computer interface is shown in Fig. 26. The various C_i and SYS signals shown are the C-register signals from the computer POT connector buffered through a power amplifier. EOMs of the form 0023XX37 were assigned to the ranging system (see SPS 37-39, Vol. III, pp. 54-65 for details of EOM structure). Octal digits 5 and 6 of this instruction are the function digits, and EOMs will be described by these octal digits in the remainder of this article. Actually, only five of the six function bits were decoded with C_{12} being left out. The decoding was done in the standard two-level fashion with C_{15} , C_{16} , C_{17} being completely decoded with 8 three-input power amplifiers and C_{14} and C_{13} with four

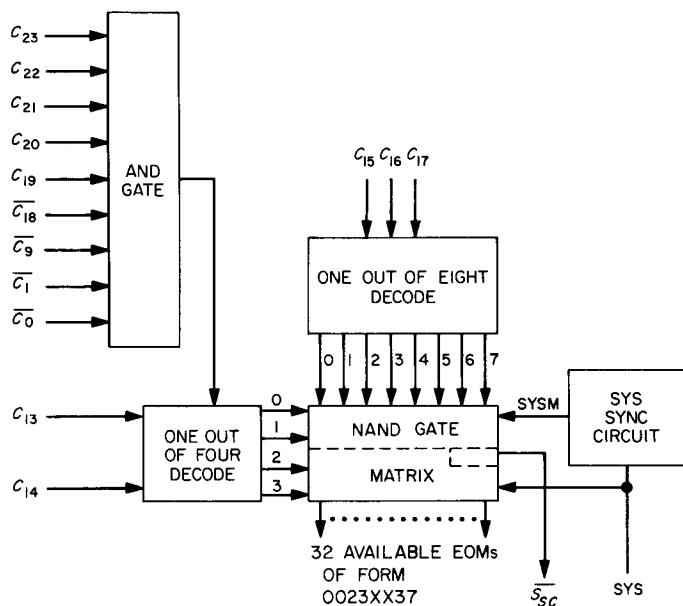


Fig. 26. Computer output interface

power amplifiers. The third input term of the C_{13} C_{14} gates was supplied with the AND function of the constant terms of the ranging system EOMs, i.e., C_{23} , C_{22} , C_{21} , C_{20} , C_{19} , \bar{C}_{18} , \bar{C}_9 , \bar{C}_1 and \bar{C}_0 . The NAND gate matrix consists of thirty-two gates with one of each of the C_{15} to C_{17} and C_{13} C_{14} terms on two of its inputs. The third leg needs the SYS signal from the computer to separate an EOM from an SKS instruction. The lower half of the matrix is supplied with SYS directly from the computer while the upper half is supplied with a SYS derived signal called SYSM. SYSM is a pulse that appears during the $4\text{-}\mu\text{s}$ SYS period but reduced to the width of, and synchronous with, the receiver clock.

Two gates of the NAND gate matrix have no SYS signal supplied and are used for SKS instructions. These are

gates 26 and 27 (octal) used to interrogate the *RF doppler loop in lock relay* and the *run-sync switch in run*, respectively. The outputs of these two gates are collector ORed and supplied to the \bar{S}_{sc} line.

c. Transmitter and receiver code generators. The transmitter code generator is clocked by a 1.000200-MHz sine wave standard from the synthesizer. The sine wave is converted to a digital clock in the shaper (see SPS 37-48, Vol. II, pp. 63-67) before clocking the coder register. The ranging sequence has five pseudo-noise components (of lengths 7, 11, 15, 19 and 23) and a clock component. Table 9 lists the feedback functions that generate each component. Note that the feedback functions for the lengths 19 and 23 components are developed in complementary form. For more detail concerning these component sequences see Ref. 2.

These five components are combined in the code function box the output of which is added modulo 2 to the clock component and delivered to the precision 50-ohm line driver (see SPS 37-48, Vol. II, pp. 63-67).

The coder function has been chosen to optimize the correlation jumps. Table 10 shows the truth table of this function of the five variables. Notice that the lengths 7 and 15 components have been developed in their complementary form. A majority function column has been added to show that there are only four discrepancies between the two truth tables. This function minimizes to

$$f = \bar{X}_{22} \bar{X}_{42} X_{62} + \bar{X}_{22} \bar{X}_{42} X_{52} + \bar{X}_{22} X_{32} X_{52} \\ + X_{32} \bar{X}_{42} X_{62} + X_{32} X_{52} X_{62} + \bar{X}_{42} X_{52} X_{62}$$

which, when factored for minimum gate count and put in the form needed for implementation by standard modules,

Table 9. Shift register feedback functions for ranging code components

Component length	Shift register length	Feedback function	Sequence
2	1	$X_{12} = \bar{X}_{11}$	01
7	3	$X_{24} = X_{22} \oplus X_{21}$	01011 10
11	5	$X_{36} = \bar{X}_{32} \bar{X}_{35} + \bar{X}_{31} \bar{X}_{41} + X_{31} X_{32} \bar{X}_{33}$	11011 10001 0
15	4	$X_{45} = X_{42} \oplus X_{41}$	10001 00110 10111
19	5	$\bar{X}_{56} = X_{51} \bar{X}_{52} X_{53} + \bar{X}_{51} X_{52} \bar{X}_{53} \\ + X_{51} X_{52} \bar{X}_{54} + \bar{X}_{51} \bar{X}_{52} X_{54} \\ + X_{52} X_{54} X_{55}$	11001 11101 01000 0110
23	7	$\bar{X}_{68} = \bar{X}_{62} X_{63} X_{65} + \bar{X}_{63} X_{64} \bar{X}_{65} \\ + X_{62} X_{64} X_{67} + \bar{X}_{61} X_{63} X_{67} \\ + X_{61} X_{62} \bar{X}_{63}$	11111 01011 00110 01010 000

Table 10. Ranging function truth table

Length 7	Length 11	Length 15	Length 19	Length 23	Ranging function	Majority function
\bar{X}_{22}	X_{32}	\bar{X}_{42}	X_{52}	X_{62}		
0	0	0	0	0	0	0
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	0	1	0	0
0	0	1	1	0	0	0
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	1	0	0
0	1	0	1	0	0	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
0	1	1	0	1	1	1
0	1	1	1	0	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	0	1	0	0
1	0	0	1	0	0	0
1	0	0	1	1	0	1
1	0	1	0	0	1	1
1	0	1	1	0	1	1
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	0	1	0	1
1	1	0	1	0	1	1
1	1	0	1	1	1	1
1	1	1	0	0	0	1
1	1	1	0	1	1	1
1	1	1	1	0	1	1
1	1	1	1	1	1	1

becomes

$$f = \bar{X}_{42} X_{62} (\bar{X}_{22} \bar{X}_{32} \bar{X}_{52}) + \bar{X}_{22} X_{32} X_{52} + \bar{X}_{22} X_{42} X_{52} + X_{32} X_{52} X_{62}$$

Other factorizations are possible but do not further reduce the gate count.

The output of the coder function is a sequence of length 1,009,470 with a period of slightly over 1 s at the transmitter clock rate. Sequences of such length are extremely difficult to verify and a malfunction of one of the gates in this function could quite easily go undetected until a critical time in a ranging operation. It is for this reason that special care was given to the factoring of the ranging function and the addition of a code function test circuit.

The test circuit consists of five switches and an AND gate capable of selecting any of the possible thirty-two combinations that the five components can assume and delivering a true level when the selected combination appears. This signal then interrogates the coder function output modulo-2 added to the selected phase of the clock component and records the answer in a flip-flop. With everything working properly, this flip-flop should remain in one state for a given switch setting and can be checked via the observation light.

A more sophisticated version of this test circuit was designed but not installed, due to space limitation, in the digital rack. This scheme replaces the switches with a digital switch and a binary counter which runs through the thirty-two states in sequence, advancing states with the 1-s time tick. The observed function bit is then transferred to the computer which compares it to a list and

signals the operator via the typewriter if a malfunction occurs. In such a scheme, each component sequence could also be monitored by the computer at the cost of one more hold register.

A series of word detectors for each component is supplied which, when ANDed together, give a sync position on the complete ranging code. This output is supplied in the receiver coder only for test purposes, but is used for coder synchronization in the transmitter.

Upon receipt of EOM 10, a flip-flop in the coder-sync control is set which allows the *next* transmitter coder word detector pulse to reset the receiver coder to the then known state of the transmitter coder. Even though this may take up to one full cycle of the sequence, it is still the most desirable method since the transmitting sequence is never interrupted and thus avoids long round-trip time delays to distant spacecraft being ranged.

It is important for the two coders to be running on the same clock when they are synchronized. For this reason, a run-sync control is provided. In the *run* position, both coders are allowed to run on their respective clocks. When synchronization is desired, however, EOM 14 sends a relay closure to the RF portion of the system which then slaves the two clocks together. EOM 13 returns the system to its normal state.

d. Receiver coder output control. This portion of the receiver coder differs from that of the transmitter since, during an acquisition, each of the six components of the full code must be correlated to the incoming sequence. Since there are seven different selections to be made, it was decided to have seven individual flip-flops, of which only one may be true at any time. Each of the seven *select* flip-flops has its set and reset inputs connected to a bit of the computer C-register and all clocks are commoned to the POT 2 signal from the computer after receipt of EOM 00. The method for selecting a desired

component, then, is for the program to deliver the correct EOM followed by a POT of the correct combination of C-register bits to do the desired selection. Table 11 gives the numbers to be outputted for each of the possible selections.

The ranging algorithm involves computing the correlation of each component for all its possible phases and then choosing the phase with the highest correlation as being correct. This function is performed by providing EOM 7 as a shift command. Upon receipt of this EOM, the component selected at that time has one clock pulse deleted, thereby dropping the phase of that component by one with respect to the received sequence. After all phases of a component have been correlated, the computer must deliver EOM 7 for *n* machine cycles, where *n* is the difference of the resulting and correct phase of the selected component.

Two phases of the selected component are supplied, one to each of the two correlator channels. These two phases, called the early and late codes, differ by one clock pulse. The two correlator channels have been designated channel 0 and channel 1. Due to the physical impossibility of constructing two identical gain correlator channels, the early and late codes are periodically switched between them to average out their differences. Two EOMs have been supplied for this purpose: EOM 11 selecting the early code for channel 0, and EOM 12 selecting the late code.

The signals delivered to the two channels of the correlator during component acquisition are $F = C_i \oplus CL$ and $F' = (C_i \oplus CL)^{-1} = C_i^{-1} \oplus CL$ where C_i and C_i^{-1} are the selected component and the selected component delayed by one, respectively, and CL is the clock component. However, these equations must be changed when the clock component itself, or the composite code, is the selected component. When the clock component is selected, the signals delivered to the two channels are

Table 11. Receiver coder component select table

Selected component	C-register bits														C-register in octal							
	C ₁₀	C ₁₁	C ₁₂	C ₁₃	C ₁₄	C ₁₅	C ₁₆	C ₁₇	C ₁₈	C ₁₉	C ₂₀	C ₂₁	C ₂₂	C ₂₃								
Clock	0	1	1	0	1	0	1	0	1	0	1	0	1	0	7	7	5	5	2	5	2	
Length 7	1	0	0	1	1	0	1	0	1	0	1	0	1	0	7	7	6	3	2	5	2	
Length 11	1	0	1	0	0	1	1	0	1	0	1	0	1	0	7	7	6	4	6	5	2	
Length 15	1	0	1	0	1	0	0	1	1	0	1	0	1	0	7	7	6	5	1	5	2	
Length 19	1	0	1	0	1	0	1	0	0	1	1	0	1	0	7	7	6	5	2	3	2	
Length 23	1	0	1	0	1	0	1	0	1	0	0	1	1	0	7	7	6	5	2	4	6	
Composite code	1	0	1	0	1	0	1	0	1	0	1	0	0	1	7	7	6	5	2	5	1	

$F = CL$ and $F' = (CL)^{-1} = \overline{CL}$. When the composite is selected, the two channels receive $F = C \oplus CL$ and $F' = (C \oplus CL)^{-1} = C^{-1} \oplus \overline{CL}$.

It can be seen from these last two sets of equations that, in these cases, the equation for the late flip-flop is simply its complement for the other cases (i.e., the true output of the early flip-flop). Thus, the function of the late code control box is to make the late flip-flop copy the early flip-flop, or its complement, as a function of the selected component.

e. One-second interrupt time routine. The remainder of the digital rack consists of special purpose counters to record events in parallel and relieve the computer from performing this duty via the interrupt lines. These counters either count or are synchronized to a third clock in the digital rack: the 500-kHz reference derived from the 1-MHz standard. This clock is delivered as a sine wave and immediately shaped to a square wave in a shaper. This digital clock is then divided by 2 to supply the basic 500-kHz signal used to control the counters and to allow any of the four quadrature phases of 500 kHz to be developed. The falling edge of the 1 MHz starts phases 1 and 3, while the falling edge of the 500 kHz defines the beginning of phase 1. The 1-s time tick from the frequency and timing subsystem (FTS) is the main source of time reference for the computer and also defines phase 1 of the four phases of the 500 kHz by the direct-set line of the 500-kHz flip-flop. The 1-s time tick is shaped and level-shifted in the shaper (see SPS 37-48, Vol. II, pp. 63-67) and also synchronized with the computer clock to serve as a correctly shaped interrupt for the computer. The 1-s time tick also freezes the counters in the digital rack, and the interrupt derived from it signals the computer to read these counters via the PIN connector.

This 1-s subroutine of the computer takes several hundred microseconds, and, if the clock doppler and UHF doppler counters are to be frozen during this time, some means must be found for counting these events during this special period. It was decided to supply both of these counters with a small auxiliary counter that accepts counts only during the 1-s time routine. This involved developing a control flip-flop, called the SEC flip-flop, that is set by the 1-s time tick at phase 1. This flip-flop remains set, then, until the computer delivers the last EOM-PIN sequence of its subroutine. This last EOM is EOM 31, *read the clock doppler counter*, and the PIN signal that follows initiates the final SEC period sequence. This sequence of pulses consists of a *phase 3 reset main*

counter pulse and a *phase 4 transfer auxiliary counters signal*, followed by the resetting of the SEC flip-flop coincident with phase 1.

f. Clock doppler counter. The clock doppler counter receives the clock doppler as a sine wave and shapes it in the shaper (see SPS 37-48, Vol. II, pp. 63-67). The rising edge of this output is then synchronized with phase 1 to develop a 0.5- μ s clock doppler signal to be sent to various counters in the digital rack. An interrupt that is synchronous with the computer clock is also developed and sent to the computer.

The phase 1 clock doppler pulse enters the 9-bit clock doppler counter via the control unit which steers it either to the main or auxiliary counter, depending upon the condition of the SEC signal. During the 1-s routine, the clock doppler counter is disabled and awaits EOM 31, which causes its output to be parallel-read into the computer via one set of PIN gates.

g. Fractional cycle counter. The fractional cycle counter reads the time interval between the receipt of the last clock doppler pulse and the 1-s time tick to the nearest 2 μ s. This is mechanized by having each clock doppler pulse reset the 15-bit fractional cycle counter (except during the 1-s routine when its value is held to be read by EOM 34).

h. Number-controlled oscillator. The NCO is a 15-bit counter with a hold register of the same length. This counter counts the 500 kHz until it reaches the *all one* state, at which time it requests reloading from the hold register. This request, called the NCO output, occurs at phase 3. The NCO hold register itself is capable of being loaded from the computer. Upon receipt of EOM 20, the hold register awaits the POT signal from the computer. The load command for the hold register must be synchronized with the 500-kHz clock to avoid trying to load both registers simultaneously. Thus, the POT 2 signal from the computer enters the POT synchronizer and develops two output signals at phases 1 and 2.

The first of these signals resets the hold register so that only single terms need be supplied to the hold register. If this were not done, one inverter per hold register bit would be needed as a reset signal for these flip-flops. The second of these signals is the clock that strobes-in the new number. Since the NCO has an output only at phase 3, interference between the loading of the hold register and loading the main counter is impossible.

An interesting minimization used in the transfer network from the hold register to the counter resulted in a requirement to program the NCO in *two's* complement form. Since the hold register is loaded into a register wired as a binary counter, the loading is done by means of the *direct set* and *direct reset* lines. However, if the binary counter is in the *all zero* position, new information can be transferred into it only via the direct set line since no carry propagations can be generated in this state. This saves the gate needed to develop the otherwise needed complementary term for the direct reset line. Waiting for the up-counter to recycle to the all zero state, however, adds one unit of time to the count; this unit can be accounted for by programming the NCO with a *two's* complement number and interpreting the proper side of the hold register as being a binary *one*.

The POT control unit merely separates the two EOM signals and delivers the POT-derived signals to the proper register.

i. Digital phase detector. The digital phase detector is a counter used to give the time measurement of the phase difference between the NCO output and the clock doppler to the nearest $2\ \mu\text{s}$. The counter is started with the receipt of a clock doppler pulse and stopped with the next NCO output. The NCO output and clock doppler pulses were chosen with different phases to avoid the simultaneous starting and stopping of this counter. Once stopped by the NCO, the digital phase detector remains off until it is read into the computer by EOM 33. After being read, the counter is reset and the control unit is allowed to await the next clock doppler pulse to repeat the cycle.

j. Ultra-high frequency doppler counter. Except for size, the UHF doppler counter is identical to the previously described clock doppler counter.

A sine wave UHF doppler signal is shaped and synchronized to phase 1. This UHF doppler signal is delivered to an 18-bit main counter or a 4-bit auxiliary counter, depending upon the status of the SEC signal. The counter is read by EOM 26, reset at the end of the SEC period by a phase 3 signal, and the auxiliary counter is then transferred to the main counter by a phase 4 signal.

The UHF doppler signal is supplied in two quadrature phases for the purpose of determining the sign of the doppler signal. The 90-deg doppler signal is shaped in

the shaper and fed to the input of a flip-flop clocked by the 0-deg doppler signal. Thus, it is determined whether the 90-deg signal is leading or lagging the 0-deg doppler, thereby determining the sign: if it leads the reference, the doppler sign is positive. This sign bit is calculated on each transition of the 0-deg doppler signal, and the constant answer is read into the computer when the magnitude is read each second. Tolerances, here, are very important. Since the maximum UHF doppler signal rate was designed to be on the order of 66 kHz, the quadrature UHF doppler signal at this rate would change within $4\ \mu\text{s}$ of the 0-deg doppler. Since it was necessary to have a phase 1 UHF doppler pulse in other parts of the system, it was decided to use this signal as a clock for the sign determination flip-flop. However, it may take as long as $2\ \mu\text{s}$ to develop this phase 1 signal after the 0-deg UHF doppler has made its transition; the $4\text{-}\mu\text{s}$ safety factor between these two signals is reduced in worst-case to $2\ \mu\text{s}$. This method does, however, guarantee the highest noise immunity possible in the circuit by avoiding clocking the sign flip-flop directly from the output of the shaper.

If it is felt that this 100% safety factor is not sufficient, the UHF doppler synchronizer can be duplicated with the 500-kHz input being replaced by 1 MHz, thus reducing the delay to a maximum of $1\ \mu\text{s}$. Space limitations, however, precluded this alternative.

k. Conclusions. The complete digital rack described above has been operating since June 1967 as a part of the *Mariner Venus 67* ranging system at the Goldstone Mars Deep Space Station. To date, all equipment has operated satisfactorily with no failures attributable either to the modules or to the design.

The various minimizations mentioned in this article were extremely desirable because of (1) the added reliability that results from fewer circuits, and (2) the large savings of circuits that was needed to meet the space allotment of one SDS 920 computer rack.

As a summary, Table 12 lists all of the EOMs used in the system.

References

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